IN THE CLAIMS

1-5. (canceled)

6. (currently amended) A buffered field effect transistor logic (BFL) level-shifting/inverter circuit comprising:

an input;

an NMOS depletion mode inverter responsive to said inverter stage input to produce an inverted output;

a buffered field effect transistor logic (BFL) stage coupled to the inverted output and comprising a first NMOS depletion mode field effect transistor (FET) having a first gate and an associated first channel, a second NMOS depletion mode FET having a second gate and an associated second channel, and a voltage drop circuit electrically connected in series between said first channel and said second channel;

a first output at an electrical node between said voltage drop circuit and said first ~~channel; and~~channel, wherein said first output is coupled to a chopping circuit configured to chop a signal based on a signal received at said first output; and

a second output at an electrical node between said voltage drop circuit and said second channel.

7. (original) A circuit in accordance with Claim 6 wherein said voltage drop circuit is a resistor.

8. (currently amended) A buffered field effect transistor logic (BFL) level-shifting/inverter circuit comprising:

an inverter stage input;

an NMOS depletion mode inverter responsive to said inverter stage input to produce an inverted output;

a buffered field effect transistor logic (BFL) stage responsive to said inverted output, said BFL stage comprising a first NMOS depletion mode field effect transistor (FET) having a first gate and an associated first channel, a second NMOS depletion mode FET having a second gate and an associated second channel; and a resistor electrically connected in series between said first channel and said second channel;

a first output at an electrical node between said resistor and said first ~~channel; and~~channel, wherein said first output is coupled to a chopping circuit configured to chop a signal based on a signal received at said first output; and

a second output at an electrical node between said resistor and said second channel, wherein said circuit is fabricated on a silicon carbide substrate.

9. (original) A circuit in accordance with Claim 8 configured to operate with a negative direct current (DC) bias on each said gate with respect to each said associated channel.

10-24. (canceled)

25. (new) A circuit in accordance with Claim 6 wherein said BFL level-shifting/inverting circuit is configured to operate with a negative direct current (DC) bias on the first gate with respect to the associated first channel and a negative DC bias on the second gate with respect to the associated second channel.